The opinion in support of the decision being entered today is not binding precedent of the Board.

Paper No. 31

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte GERMANO NICOLLINI and ANGELO NAGARI

Appeal No. 2000-1939
Application 08/791,281

ON BRIEF

Before MARTIN, GROSS, and LEVY, Administrative Patent Judges.

MARTIN, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 16-34 and 36-38, all of the pending claims, under 35 U.S.C. § 103(a). We reverse.

The invention

The invention is an improvement in a prior art switched capacitor integrator of the type shown in Appellants' Figure 1, which includes a first switched capacitor C2 connected between switches SW1 and SW2 and a second switched capacitor C3 connected between switches SW3 and SW4, the switches being controlled by the waveforms shown in Figure 2:

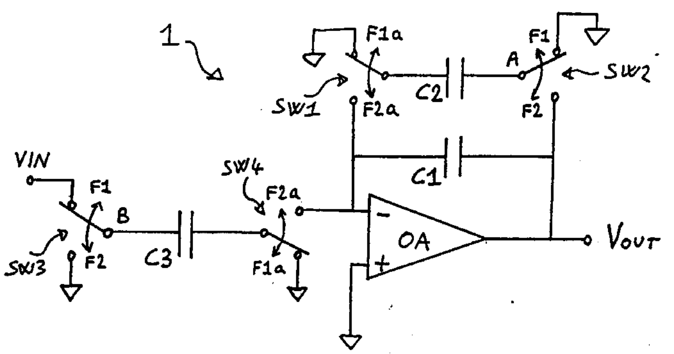


FIG 1 (Prior Art)

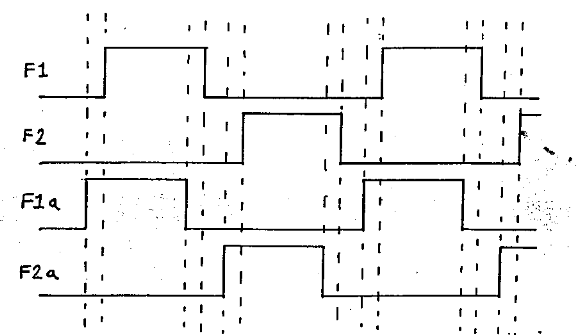


FIG 2 (Prior Art)

During the overlapping portions of clocking pulses F1 and F1a, switches SW1-SW4 are in the positions shown in Figure 1, in which capacitor C3, for example, is connected between VIN and ground. During the overlapping portions of clocking pulses F2 and F2a, capacitor C3 will be connected between the negative amplifier input terminal and ground. As shown in Figure 3, reproduced below, switch SW3 consists of transistors M1 and M2 and switch SW4 consists of transistors M3 and M4. Switches SW1 and SW2 presumably are constructed in the same way.

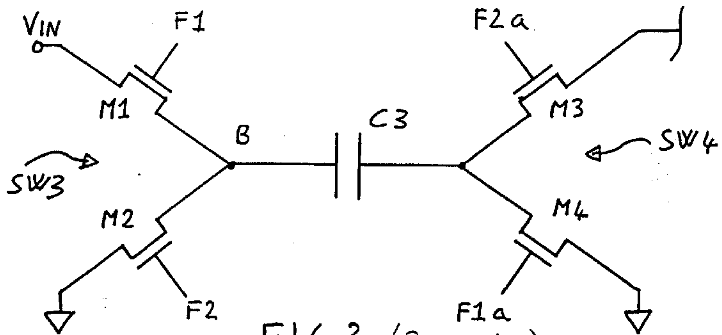


FIG 3 (Prior Art)

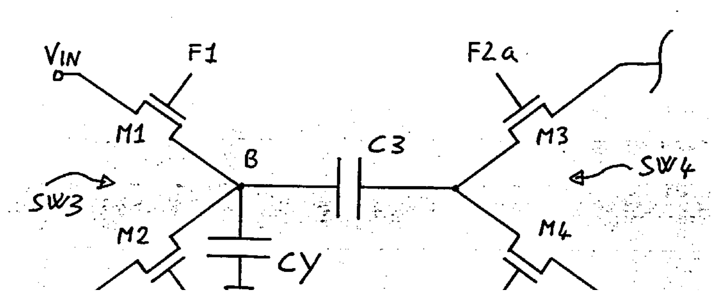
This prior art switching circuitry suffers from harmonic distortion caused by current injection occurring during the turning off of transistor M4, as explained <u>infra</u>. This is not a problem during the turning off of transistors M1-M3 for the following reasons. When transistor M1 is turned off, transistor M4 is already off, with the result that no current can be injected from transistor M1 into the floating capacitor. Specification at 3, lines 29-34. Likewise, when transistor M2 is turned off, transistor M3 is already off. <u>Id.</u> Although transistor M3 is turned off while transistor M2 is still on, thereby causing charge to be injected from transistor M3 into capacitor C3, the amount of injected current is fixed and thus causes some voltage offset but no harmonic distortion. <u>Id.</u> at 4, lines 4-5 and 12-15. The reason is that "the voltage across M3 is fixed (virtual ground of an operational amplifier) and the other end of the capacitor C3 is also connected to a fixed (ground) voltage reference via the transistor M2, which transistor is still in a conduction state." Id. at 4, lines 6-11.

In contrast, when transistor M4 is turned off, which occurs while transistor M1 is still on, the charge stored in the channel of transistor M4 is injected into capacitor C3 in an amount that is dependent on the magnitude of the input voltage VIN. Id. at 4, lines 15-21. More particularly,

> [t]he circuit node B sees, toward ground, an intrinsic parasitic capacitance Cp which is due to the source and drain diffusions of the two transistors M1 and M2, and a conduction resistance RON of the transistor M1.
>
> As those familiar with the art will readily recognize, both the capacitance Cp and the resistance RON have a non-linear pattern versus voltage.
>
> Since the voltage at the circuit node B varies with the voltage of the input signal VIN, it follows that the impedance seen toward ground from the circuit node B, and consisting of a parallel of the parasitic capacitance Cp and the conduction resistance RON of the transistor M1, will also vary with the input voltage.
>
> This causes the amount of the charge injected into the capacitor C3 by the transistor M4 to be non-constant and vary with the input signal Vin [sic, VIN], thereby adversely affecting the system linearity and introducing harmonic distortion in the output signal.

Id. at 4, line 22 to page 5, line 3.

Appellants' solution, shown in Figure 7, reproduced below, is to connect an additional capacitance CY which between the common terminal (node B) of switch SW3 and ground.



The specification explains that

> [b]y suitably sizing the capacitor CY so that its capacitance is much higher than the parasitic capacitance Cp of the node B and that its equivalent impedance is much lower than the conduction resistance Ron of the transistors at a frequency equal to the inverse of the decay time of the clocking signals used to drive the switch transistors, the overall impedance as seen from the circuit node B toward ground can be linearized.

Id. at 8, lines 26-33. As a result, the amount of charge injected into capacitor C3 by transistor M4 when it turns off is constant, thereby resulting in a constant voltage offset in the output signal but no system harmonic distortion. Id. at 10, lines 13-24.

Figure 6, reproduced below, shows this technique, using capacitors CX and CY, applied to nodes A and B of the switched capacitors C2 and C3 in a circuit of the type shown in prior art Figure 1.

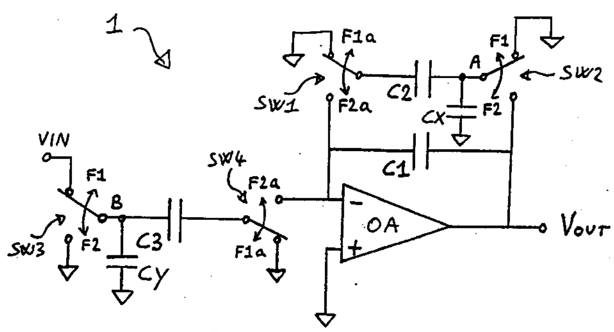


FIG 6

Figures 4 and 5, not reproduced below, show this technique applied to two alternative embodiments each having a single switched capacitor.

The claims

Claim 34, which is representative, reads as follows:[1]

34. A switched capacitor circuit with low distortion having a circuit input terminal, the circuit comprising:

a first switching element with a first switch terminal coupled to the circuit input terminal and a second switch terminal coupled to a reference level, a switch common terminal, and a switch control to alternatively couple said switch common terminal to said first switch terminal or said second switch terminal at a predetermined switching rate, said first switching element having a nonlinear parasitic

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[1] Claim 34 is incorrectly reproduced in the Appendix; the term "nonlinear" should not be hyphenated. We note too that claim 18 as it appears in the application and the Appendix incorrectly depends on itself.

capacitance from said switch common terminal to said reference level and a nonlinear conduction resistance from said first switch terminal to said switch common terminal when said switch control couples said first switch terminal to said switch common terminal, said nonlinear parasitic capacitance and said nonlinear conduction resistance forming a nonlinear impedance from said switch common terminal to said reference level; and

a compensation capacitance coupled from said switch common terminal to said reference level to linearize said nonlinear impedance from said switch common terminal to said reference level, wherein said compensation capacitance has a capacitance value larger than said parasitic capacitance and an impedance lower than said conduction resistance at said predetermined switching rate.

The rejection

The rejection is based on the admitted prior art circuit shown in Appellants' Figure 1 in view of the following U.S. Patent:

Gregorian et al. (Gregorian) 4,393,351 July 12, 1983

All of the appealed claims stand rejected under 35 U.S.C. § 103 for obviousness over the admitted prior art in view of Gregorian.

The merits of the rejection

Gregorian's Figure 3, reproduced below, shows an integrator in which one and only one terminal of a feedback capacitor 23 is switched, the other terminal being permanently connected to the negative input terminal of operational amplifier 19. Switching is effected by transistor switches 24 and 26 in response to clock signals ϕ_2 and ϕ_3 , shown in Figure 4, also reproduced below.

FIG. 3

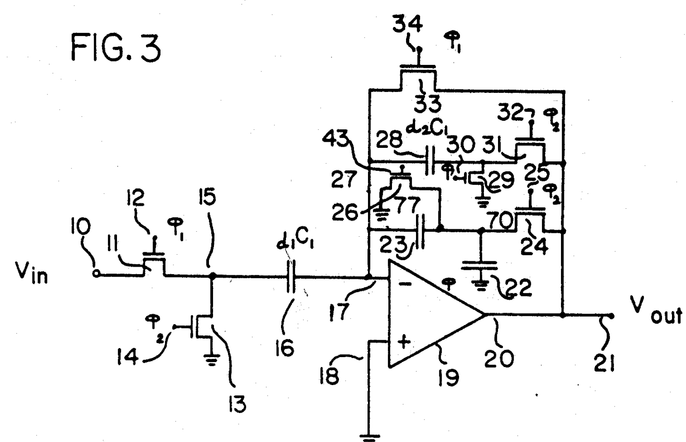
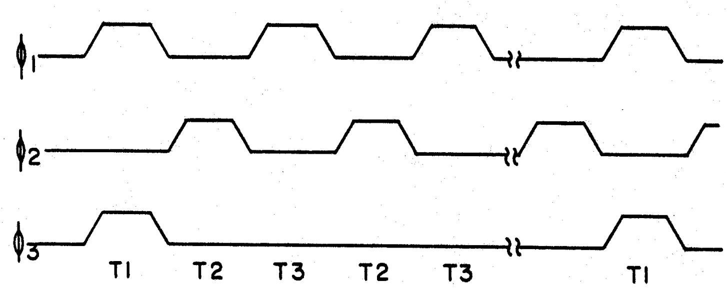


FIG. 4



Specifically, switch 26 is closed at time T1 in response to each positive-going pulse of clock signal ϕ_3, whose frequency is about

1/1000 of the frequency of complementary clock signals ϕ_1 and ϕ_2, thereby connecting the capacitor terminal to ground and discharging the capacitor to reinitialize the integrator (col. 4, l. 42 to col. 5, l. 9). During time T2, clock signal ϕ_3 goes low, opening switch 26, and clock signal ϕ_2 goes high, closing switch 24 (col. 5, ll. 29-34), thereby connecting the switched capacitor terminal to output terminal 21 of operational amplifier 19.

At time T3, ϕ_2 goes low, opening switch 24 (col. 5, ll. 53-54). However,

> [d]uring the periods when ϕ_2 is low and thus switch 24 is off, leakage currents through switch 24 tend to discharge capacitor 23. By the use of capacitor 22 connected to node 70, capacitor 22, as well as capacitor 23, is partially discharged due to the leakage currents through non-conducting switch 24. By the proper sizing of capacitor 22, the effect of leakage currents through switch 24 on the charge stored on capacitor 23 will be negligible. . . . Thus, the inclusion of capacitor 22, while not absolutely necessary, improves the accuracy of the integrator stage by minimizing the effect of leakage currents on integration capacitor 23.

Gregorian, column 6, lines 8-30.

The examiner's position is that it would have been obvious to incorporate Gregorian's capacitor 22 in the admitted prior art circuit shown in Appellants' Figure 1 "for the purpose of minimizing the effect of leakage current in the first impedance (capacitors C2 & C3)." Answer at 5.[2] Nevertheless, we agree with Appellants that Gregorian would not have suggested to the artisan that the admitted prior art circuit suffers from the problem of capacitor discharge due to a leakage current from one or more of the switching transistors. Although, as the examiner correctly notes (Answer at 7-8), the admitted prior art circuit and Appellants' circuit are similar in that both include a capacitor having a terminal connected to two switches, the circuits are otherwise considerably different in structure and operation as regards the capacitors in question. Specifically, in the admitted prior art circuit both of the terminals of the capacitor are switched by switches operating at the fundamental clocking frequency (Fig. 2), whereas in Gregorian only one of the terminals of capacitor 23 is switched at all, let alone at the fundamental clocking frequency (i.e., by transistor 24 in response to signal ϕ_2). In view of these significant differences, we are not persuaded that one skilled in the art

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[2] As the examiner correctly notes (Answer at 6), a proper § 103(a) rejection need not be based on solving the same problem that is solved by the applicant's invention. See In re Beattie, 974 F.2d 1309, 1312, 24 USPQ2d 1040, 1042 (Fed. Cir. 1992) ("As long as some motivation or suggestion to combine the references is provided by the prior art taken as a whole, the law does not require that the references be combined for the reasons contemplated by the inventor. In re Kronig, 539 F.2d 1300, 1304, 190 USPQ 425, 427-28 (CCPA 1976); In re Lintner, 458 F.2d 1013, 1016, 173 USPQ 560, 562 (CCPA 1972).").

would have assumed that the capacitor discharge problem recognized and solved by Gregorian also exists in the admitted prior art circuit.

The rejection of the appealed claims based on the admitted prior art in view of Gregorian is therefore reversed.

REVERSED

JOHN C. MARTIN Administrative Patent Judge	)	
ANITA PELLMAN GROSS Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
STUART S. LEVY Administrative Patent Judge	)	

JCM/sld

cc:

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